29. (new) A method according to claim 28, further comprising:

simultaneously forming (i) a storage node of the cell capacitor, (ii) an additional storage node of the additional cell capacitor, (iii) the lower electrode of the capacitor element, and (iv) an additional lower electrode of the additional capacitor element;

simultaneously forming (i) a dielectric layer of the cell capacitor, (ii) an additional dielectric layer of the additional cell capacitor, (iii) a dielectric layer of the capacitor element, and (iv) an additional dielectric layer of the additional capacitor element; and

simultaneously forming (i) a cell plate of the cell capacitor and the additional cell capacitor, (ii) an upper electrode of the capacitor element, and (iii) an additional upper electrode of the additional capacitor element.--

REMARKS

Applicant has amended claim 1, canceled claims 5-14 without prejudice, and added new claims 17-29. Claims 1-4 and 15-29 are currently pending. Reexamination and reconsideration are respectfully requested.

A minor amendment was made to claim 1 for clarity and not in response to any rejection. Claims 5-14 have been canceled without prejudice as non-elected claims.

In the specification, applicant has amended the paragraph starting on page 1, line 6, to insert the serial numbers of the cited applications.

Claims 1-4 and 15-16 were rejected under 35 U.S.C. 103(a) as unpatentable over Ohyu et al (US 6,291847) in view of Lee et al (US 6,215,142), Choi et al (U.S. 6,040,596) and Takada et al (U.S. 6,110,772). The rejection is respectfully traversed.

To establish a prima facie case of obviousness, the following criteria should be met. First, there should be a suggestion or motivation in the art to modify the reference or to combine reference teachings. Second, there should be a reasonable expectation of success. Third, the reference(s) must teach all the claim limitations. MPEP section 706.02(j). Applicant respectfully submits that the Examiner's citations to the art are insufficient to satisfy the three criteria above and accordingly, the rejections should be withdrawn.

In rejecting the claims, the Examiner stated that "it is well established in the art that certain process features can be 'simultaneously' formed during a process sequence. For example,

forming a cell plate and a resistance element simultaneously is relatively routine in processing. In like manner, formation of dielectric layers (simultaneously) in different locations is also well established in the art. It would have been obvious to one of ordinary skill to simply combine Lee et al. Choi et al. and Takada et al. with Ohyu et al. . ."

Applicant notes that the Examiner did not cite any specific art to support the above contentions. In addition, the Examiner cited no specific portion of the art that describes or suggests the "simultaneous forming" recited in all of the elements of the claims. For example, claim 1 recites in part:

> *(a) simultaneously forming a well and an impurity region that is used to electrically connect a lower electrode of the capacitor element and another semiconductor element, wherein the well is located in the semiconductor substrate in the DRAM region, and the impurity region is located in the semiconductor substrate in the analog element region;*
>
> *(b) simultaneously forming a storage node of the cell capacitor and the lower electrode of the capacitor element;*
>
> *(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and*
>
> *(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.*

Applicant respectfully submits that the Examiner cited no reference that suggests that it is conventional in the art to simultaneously form all of the features as set forth in the recited methods. That the simultaneous formation of certain types of layers may in general be known does not establish that the simultaneous formation of the features recited in the claims is known. Given the number of layers and regions in certain types of semiconductor devices, applicant respectfully submits that there are numerous combinations of layers which could be formed at various times. The recited features are formed in a particular manner to achieve particular advantages as described in the specification. Applicant respectfully submits that the Examiner cited no specific portions of references that set forth all of the recited claim elements. Accordingly, the rejection is deficient and should be withdrawn.

In addition, the Examiner has cited no portion of the art that suggests the combination of references proposed by the Examiner. That one could possibly combine the references does not provide adequate suggestion for combining the references as suggested by the Examiner. Applicant respectfully submits that the Examiner is using improper hindsight to attempt to combine the references. As noted above, even if combined, the Examiner cited no portion of the art the describes the recited claim elements.

Accordingly, for at least the above reasons, applicant respectfully submits that the rejection of claims 1-4 should be withdrawn.

Claims 15-16 can be distinguished at least in a similar manner to claims 1-4.

Applicant has added new claims 17-29. Support for the new claims may be found throughout the specification and in the original claims. It is believed that no new matter has been entered.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-4 and 15-29 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on January 3, 2003.

Alan S. Raynes — January 3, 2003

Alan S. Raynes — **(Date)**

Version With Markings to Show Changes Made

The paragraph in the specification starting at page 1, line 6, was amended as follows:

Japanese patent application no. 2000-5336, filed January 14, 2000, is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/759,665 [_____, filed on January 13, 2001, entitled "Methods for Manufacturing Semiconductor Devices and Semiconductor Devices," invented by Hiroaki Tsugane and Hisakatsu Sato, docket no. 15.28/5628,] is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/759,666 [_____, filed on January 13, 2001, entitled "Semiconductor Devices and Methods for Manufacturing the Same," invented by Hiroaki Tsugane and Hisakatsu Sato, docket no. 15.29/5629,] is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/759,915 [_____, filed on January 13, 2001, entitled "Semiconductor Devices and Methods for Manufacturing the Same," invented by Hiroaki Tsugane and Hisakatsu Sato, docket no. 15.30/5630,] is hereby incorporated by reference in its entirety.

Claim 1 was amended as follows:

1. (amended) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a well and an impurity region that is used to electrically connect a lower electrode of the capacitor element and another semiconductor element, wherein the well is located in the semiconductor substrate in the DRAM region, and the impurity region is located in the semiconductor substrate in the analog element region;

(b) simultaneously forming a storage node of the cell capacitor and the lower electrode of the capacitor element;

(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.